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| **Course Name:** | **Digital Design Laboratory** | **Semester:** | **III** |
| **Date of Performance:** | **09/ 09 / 24** | **Batch No:** | **C3** |
| **Faculty Name:** | **Bharathi Narayan** | **Roll No:** | **16010123217** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **\_\_\_/25** |

**Experiment No: 7**

**Title: Asynchronous Counter**

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| **Aim and Objective of the Experiment:** |
| To design and implement 3 bit Asynchronous up counter using JK Flip Flop |

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| **COs to be achieved:** |
| **CO3**: Design synchronous and asynchronous sequential circuits. |

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| **Tools used:** |
| Trainer kits |

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| **Theory:** |
| **Circuit diagram of 3 bit Asynchronous Up counter using JK FF (IC 7476)**  **Pin diagram of JK FF (IC 7476)** |

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| **Implementation Details** |
| **Procedure**   1. Locate IC 7476 JK FF on Digital trainer kit 2. Apply various inputs to appropriate pins as per the circuit diagram of the 3 bit Asynchronous up counter with reference to the pin configuration of the IC. 3. Make sure of Reset and Clear Pins connections with reference to data sheet information. 4. Connect a pulsar switch to the clock input. 5. Verify the working and prepare a truth table. |
| **Post Lab Subjective/Objective type Questions:** |
| 1. How JK FF need to be configured to use for counter operation?   Ans. To configure a JK flip-flop (FF) for counter operation:   * Clock input: Provide the clock signal to trigger the flip-flop. * Use multiple JK FFs: For counters (e.g., binary counters), connect the Q output of one flip-flop to the clock input of the next flip-flop in the series. * J = K = 1: This makes the JK flip-flop toggle its state on every clock pulse.  1. What changes are required to use the same counter as 3 bit asynchronous down counter?   Ans.  To use the same counter as a 3-bit asynchronous down counter, follow these steps:   * Invert the Q output: Connect the inverted output (Q') of each JK flip-flop to the clock input of the next flip-flop, instead of the Q output. * J = K = 1: Keep J = K = 1 to maintain the toggling behavior on each clock pulse. * Clock input: Provide the clock signal to the first flip-flop, which triggers the rest in sequence.  1. Draw the timing diagram of 3 bit Asynchronous up counter.   Ans.   1. What is mod n concept used in counters?   Ans. Counters whose values “wrap around” back to zero when they reach the value n are called modulo-n counters. The most common example is a modulo-10 counter that counts from 0 up to 9 and then “wraps around” back to 0.   1. For Mod-5 counter how many JK FFs are required?   Ans. The number of flip flops required for mod 5 is 3 because it is in between mod 4 and mod 8. |
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| **Conclusion:** |
| By performing this experiment I learnt how to use JK flip flops |

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| **Signature of faculty in-charge with Date:** |